Vertical Interconnects for Stacked ASICs in Soft Encapsulant

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Introduction

Microchannel Neural Interfaces

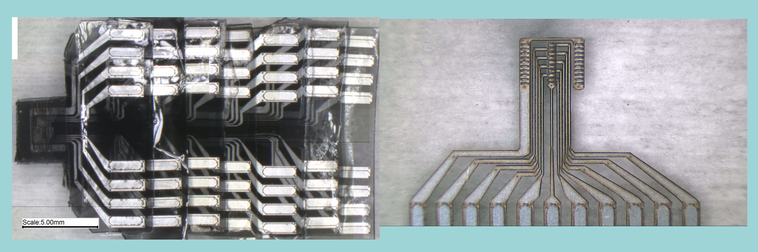
High selectivity nerve recording requires close proximity between implanted recording devices and nerve tissues. One such device is the microchannel neural interface (MNI), which comprises an array of *circa* 100 µm diameter holes through which a peripheral nerve will regrow. These microchannels are electrically insulating with three electrodes along the length. With the axons thus confined, the action potentials produce large (~100µV) signals with low cross-talk and recordings are independent of the positions of the Nodes of Ranvier. 3-dimensional MNIs have been manufactured by several methods including laminating layers, each comprising metal foil, cut to form the electrodes and interconnect, with silicone insulator [1,2].

The Interconnection Limit

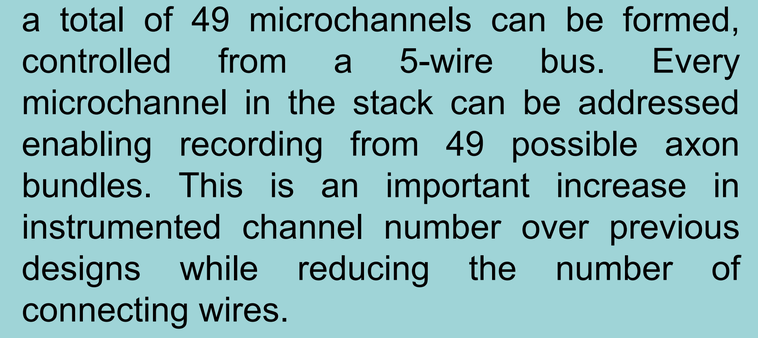
The number of microchannels is limited because each requires at least one connecting wire. Replacing the passive conductor layer with an active ASIC will allow channel selection and signal multiplexing using a small number of bus lines.

In this manner an MNI comprising 7 layers and a total of 49 microchannels can be formed, controlled from a 5-wire bus. Every microchannel in the stack can be addressed enabling recording from 49 possible axon bundles. This is an important increase in instrumented channel number over previous designs while reducing the number of connecting wires.

Forming a connection between vertically arranged ASICs suitable for implantation is a challenge. This poster describes one approach and presents a manufactured prototype.



Stacking passive MNIs: 7 layers, 49 channels, 56 pads required (left); 1 layer, 10 channels, 11 pads required (right).



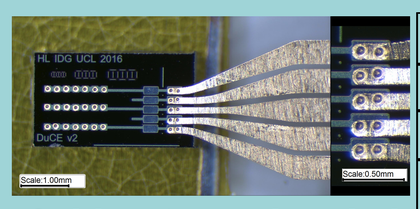
The proposed solution: stacked active ASICs with 5 bus lines.

Methods

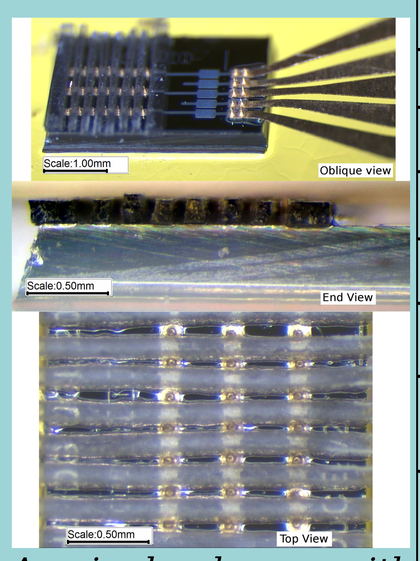
The Vertical Parallel Bus

We have designed an interconnect system for stacked silicon ASICs in a silicone conformal layer encapsulant [3]. Laser patterned metal ribbon structures were electrical rivet bonded to ASIC pads [4]. ASICs were encapsulated with a thin layer of silicone by spin coating. Microchannels were formed in a separate silicone layer using an Nd:YAG laser as previously described [1]. Microchannels were aligned and bonded to ASICs using a thin layer of spin coated silicone.

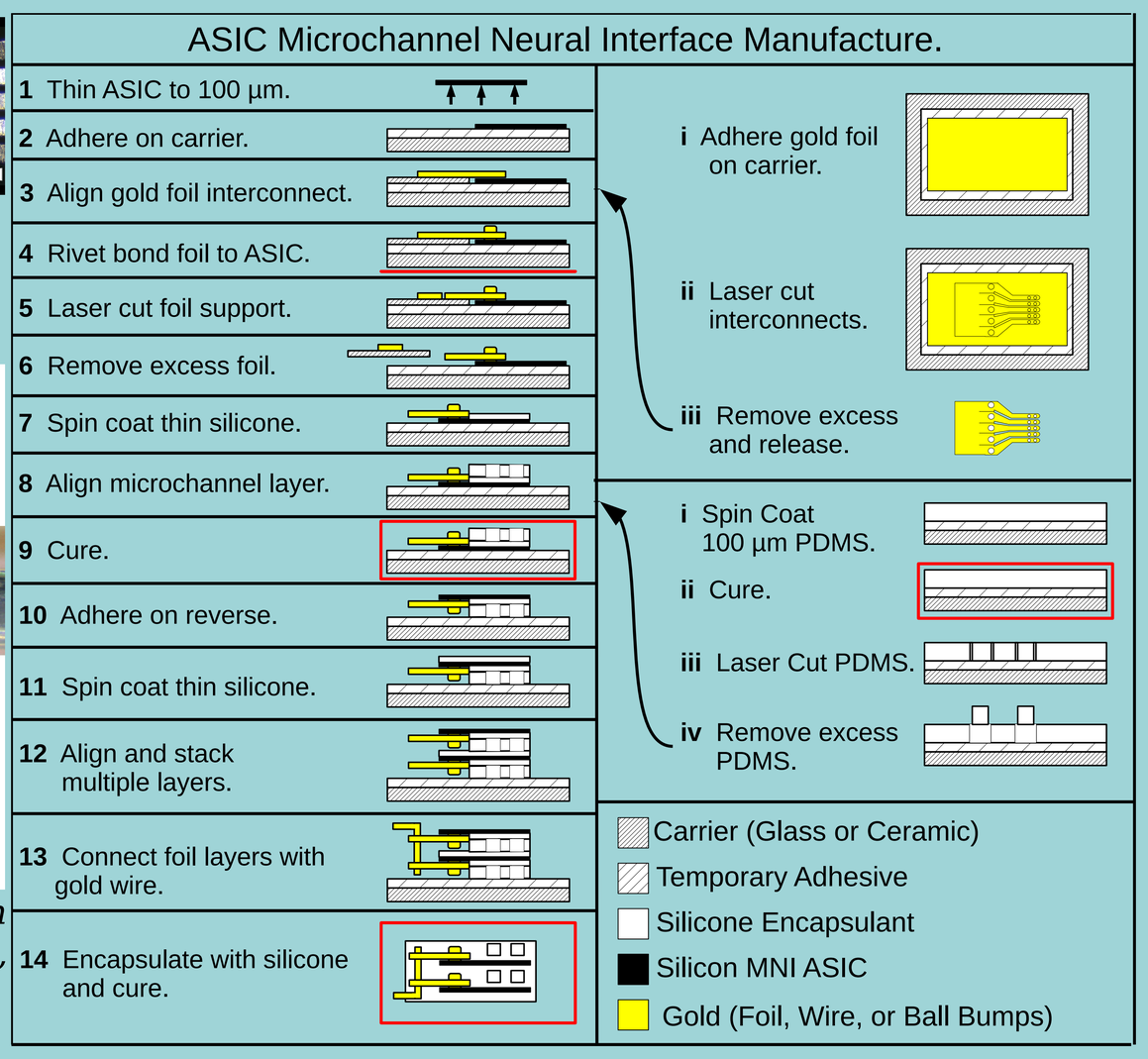
ASIC-microchannel layers were stacked using silicone adhesive. Wire was fed through holes in vertically arranged ribbons to form an interconnect, connecting the stacked ASICs as a parallel electrical bus. Conductive epoxy resin (EpoTek H20E) was used to connect layers in this design, however future work will use implantable methods e.g. low temperature solder. The rivet bonds withstood forces applied during manufacture, including spin-coating steps at >4000 rpm. In this prototype ASICs were 500 µm thick, in future ASICs will the thinned to 100 µm prior to processing [4], The prototype contained 3 layers, future designs with 7 layers may improve vertical interconnect manufacture by supplying additional support for the vertical wires.



Gold rivet bonded foil interconnect, a single ASIC layer.



A single layer with ASIC, interconnects, and microchannels.



Discussion

Prototyping indicates that the interconnects described can be manufactured in a straightforward manner. We aim to test such an MNI on regenerated nerve to show that it can both stimulate and record neural activity. We are also investigating the materials aspects of using integrated circuits in intimate contact with body fluid to see what device lifetime may be possible (see posters from Lamont *et al.* and Shah Idil *et al.*).

Laser cut gold foil (above), and a prototype before (above-right) and after (right) silicone encapsulation.

References

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4. Giagka, V., Vanhoestenberghe, A., Donaldson, N. & Demosthenous, A. Evaluation and optimization of the mechanical strength of bonds between metal foil and aluminium pads on thin ASICs using gold ball studs as micro-rivets. *Proceedings of the 5th Electronics System-integration Technology Conference* (2014).

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